AP-01-002B

October 24, 2003

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject:	Serial No. 10/627,834 07/25/03
	Peter W. Lee et al.
	A NOVEL SET OF 3-LEVEL CONCURRENT WORDLINE BIAS CONDITIONS FOR NON-VOLATILE SEMICONDUCTOR ONE-TRANSISTOR-CELL, NOR-TYPE FLASH EEPROM MEMORY ARRAY
	Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313,1450, on October 27, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 10/27/03

U.S. Patent 5,748,538 to Lee et al., "Or-Plane Memory Cell Array for Flash Memory with Bit-Based Write Capability, and Methods for Programming and Erasing the Memory Cell Array," discloses a memory cell array of a flash electrically erasable programmable read only memory (EEPROM) .

U.S. Patent 5,464,998 to Hayakawa et al., "Non-Volatile Semiconductor Memory NAND Structure with Differently Doped Channel Stoppers," discloses a non-volatile semiconductor memory device including NAND type memory cells arranged in a matrix pattern over a semiconductor substrate and channel stopper layers, provided on the substrate, for separating adjacent NAND type memory cells.

U.S. Patent 5,848,000 to Lee et al., "Flash Memory Address Decoder with Novel Latch Structure," discloses a flash memory address decoder including a plurality of voltage terminals to receive a plurality of voltages, an address terminal to receive a plurality of address signals and a procedure terminal to receive a procedure signal.

U.S. Patent 6,038,170 to Shiba, "Semiconductor Integrated Circuit Device Including a Plurality of Divided Sub-Bit Lines," describes NAND-type flash EEPROMs.

U.S. Patent 5,708,600 to Hakozaki et al., "Method for Writing Multiple Value into Nonvolatile Memory in an Equal Time," provides a method for writing a multiple value into a nonvolatile memory capable of writing multiple value data into a floating gate type memory cell in an equal time even when the data are varied.

The following four U.S. Patents describe ETOXTM flash cell operations:

1) U.S. Patent 5,712,815 to Bill et al., "Multiple Bits Per-Cell Flash EEPROM Capable of Concurrently Programming and Verifying Memory Cells and Reference Cells."

2) U.S. Patent 5,790,456 to Haddad, "Multiple Bits-Per-Cell Flash EEPROM Memory Cells with Wide Program and Erase VT Window."

3) U.S. Patent 6,011,715 to Pasotti et al., "Method for Multilevel Programming of a Nonvolatile Memory, and a Multilevel Nonvolatile Memory."

4) U.S. Patent 5,825,689 to Wakita, "Nonvolatile Semi-conductor Memory Device Having Data Detecting Circuit for Memory Cells Block."

The following seven U.S. Patents describe ANDTM flash cell's operations in detail:

1) U.S. Patent 6,072,722 to Hirano, "Method of Driving a Nonvolatile Semiconductor Storage Device."
2) U.S. Patent 6,101,123 to Kato et al., "Nonvolatile Semiconductor Memory with Programming and Erasing Verification."
3) U.S. Patent 5,892,713 to Jyouno et al., "Nonvolatile Semiconductor Memory Device."
4) U.S. Patent 6,009,016 to Ishii et al., "Nonvolatile Memory System Semiconductor Memory and Writing Method."
5) U.S. Patent 5,982,668 to Ishii et al., "Nonvolatile Memory System, Semiconductor Memory and Writing Method."
6) U.S. Patent 5,959,882 to Yoshida et al., "Nonvolatile Semiconductor Memory Device and Data Writing Method Therefor."
7) U.S. Patent 5,757,699 to Takeshima et al., "Programming Which Can Make Threshold Voltages of Programmed Memory Cells Have a Narrow Distribution in a Nonvolatile Semiconductor Memory."

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

FORM PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
AP-01-002 B	10/627,834
Applicant: Peter W. Lee et al.	
Filing Date: 07/25/03	Group Art Unit:

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5464998	11/7/95	Hayakawa et al.	257	316	3/31/94
	5748538	5/5/98	Lee et al.	365	185.06	11/14/96
	5712815	1/27/98	Bill et al.	365	185.03	4/22/96
	5790456	8/4/98	Haddad	365	185.17	5/9/97
	5844800	12/8/98	Lee et al.	365	185.23	3/18/97
	6038170	3/14/00	Shiba	365	185.13	2/2/99
	6011715	1/4/00	Pasotti et al.	365	185.03	11/3/98
	5825689	10/20/98	Wakita	365	185.11	9/5/97
	6072722	6/6/00	Hirano	365	185.13	7/8/98
	6101123	8/8/00	Kato et al.	365	185.11	4/8/99
	5892713	4/6/99	Iyouno et al.	365	185.11	2/23/96

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through

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	6009016	12/28/99	Ishii et al.	365	185.24	6/2/99
	5982668	11/9/99	Ishii et al.	365	185.24	8/18/98
	5959882	9/28/99	Yoshida et al.	365	185.03	7/9/97
	5757699	5/26/98	Takeshima et al.	365	185.24	6/3/97
	5708600	1/13/98	Hakozaki et al.	365	185.03	10/1/96

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